

	L #	Hits	Search Text	DBs
1	L2	34	((detect\$3 determin\$3 diagnos\$3 identif\$6) near10 instruction) near99 ((configuration adj2 (data memory))) and cpu	USPAT; US-PGPUB
2	L1	34	((detect\$3 determin\$3 diagnos\$3 identif\$6) near10 instruction) near99 ((configuration adj2 (data memory))) and cpu	USPAT; US-PGPUB

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	Docum ent ID	U	Title	Current OR
1	US 20040 02512 1 A1	<input type="checkbox"/>	Method of and apparatus for information processing	716/3
2	US 20040 00322 3 A1	<input checked="" type="checkbox"/>	Apparatus and method to decrease boot time and hibernate awaken time of a computer system	713/1
3	US 20030 20479 1 A1	<input checked="" type="checkbox"/>	Rules-based configuration problem detection	714/48
4	US 20030 05612 8 A1	<input checked="" type="checkbox"/>	Apparatus and method for a selectable Ron driver impedance	713/300
5	US 20030 03687 4 A1	<input checked="" type="checkbox"/>	Network-based system for configuring a measurement system using configuration information generated based on a user specification	702/123
6	US 20030 00510 4 A1	<input checked="" type="checkbox"/>	Server configuration tool	709/223
7	US 20020 15706 6 A1	<input checked="" type="checkbox"/>	Reconfigurable processor devices	716/1
8	US 20020 13369 0 A1	<input checked="" type="checkbox"/>	Semiconductor integrated circuit	712/34
9	US 20020 01667 4 A1	<input checked="" type="checkbox"/>	Golf course yardage and information system having improved zone information and display characteristics	701/215
10	US 20020 01194 9 A1	<input checked="" type="checkbox"/>	Golf course yardage and information system with zone detection	342/357 .06
11	US 20020 01054 4 A1	<input checked="" type="checkbox"/>	Display monitor for golf cart yardage and information system	701/213
12	US 67287 23 B1	<input checked="" type="checkbox"/>	Method and system for verifying configuration transactions managed by a centralized database	707/102
13	US 65976 66 B1	<input checked="" type="checkbox"/>	Method, editor, computer, control module, and storage means for editing configuration data for telecommunications systems	370/254
14	US 65533 95 B2	<input checked="" type="checkbox"/>	Reconfigurable processor devices	708/232
15	US 65256 90 B2	<input checked="" type="checkbox"/>	Golf course yardage and information system with zone detection	342/357 .13
16	US 64702 42 B1	<input checked="" type="checkbox"/>	Display monitor for golf cart yardage and information system	701/1
17	US 64218 17 B1	<input checked="" type="checkbox"/>	System and method of computation in a programmable logic device using virtual instructions	716/16
18	US 63538 41 B1	<input checked="" type="checkbox"/>	Reconfigurable processor devices	708/232
19	US 63517 97 B1	<input checked="" type="checkbox"/>	Translation look-aside buffer for storing region configuration bits and method of operation	711/207

GWA fields from the control store 36 are applied as the selection inputs to the multiplexer 77 and 78 respectively. Additionally, a write enable flip-flop 79 responds to timing signals to and 150, which timing signals will be later described, applies control signals to the chip enable inputs of the multiplexers 77 and 78 to provide the timing for the GRS writing and reading operations.

In a manner to be further described hereinafter, the CPU 10 operates with a 100 nanosecond micro cycle, timing strobes being provided every ten nanoseconds, the strobes being designated as to-190. Thus, it is appreciated that at the write enable flip-flop 79 is set and at 150 it is reset. Thus, during the first half of the micro cycle the multiplexer 78 is enabled for writing and during the second half of the micro cycle the multiplexer 77 is enabled for reading. Thus, in accordance with the GWA and GWA fields from the micro instruction words, one of the four input addresses is selected by the GWA field during the first half of the micro cycle and is transmitted through the OR gate 76 to address the GRS 32 for writing. During the second half of the micro cycle one of the four input addresses is selected by the GWA field and transmitted through the OR gate 76 to address the GRS 32 for reading.

configuration 76 to address the GRS 32 for reading. RA1 usually contains the absolute address of the register pointed at by the field of the macro instruction, which value is generally computed toward the beginning of the macro instruction emulation by the local processor 27. The RA1 register receives this address from the 7 least significant bits from the D4 bus 30. The RA2 register is usually utilized to contain the address of $A_0 + 1$ for the 1108 double precision instructions and receives this address information from the 7 least significant bits of the D4 bus 30. The register RA3 usually contains the GRS address provided by the u field of the macro instruction which, in accordance with 1108 address, is the "hidden" memory. Any of the local processors 17, 18 and 19 may provide the computations to provide this address information to RA3 which is taken from the right 7 of the left 20 bits of the 40-bit wide D bus 23. The fourth address source is provided directly from the macro instruction register 13 by the x field concatenated with the D6 bit. D6 determines whether the x register is in the user state or in the execute state in a manner identical to that utilized in the 1108. Because of the boundaries chosen by the 1108, the D6 bit can merely be concatenated in a manner to be described hereinafter.

The addressing for the GRS was generally discussed above with respect to Tables 3 and 9 from which it is appreciated that the base address computations are performed by the local processor 27 in response to the GWA field from the IST memory 38, the results being provided to the register address registers 33 as directed by the GWA and GWA fields in the micro instructions in the control store 36.

As previously discussed, the CPU 10 includes local processors 17, 18 and 19 designated as P1, P2 and P3 which have local memories 24, 25 and 26 associated therewith respectively. Each of the local memories 24, 25 and 26 are 64 words long by 40 bits wide. The local memory 24 is addressed by a 6-bit, 3 input multiplexer 80 where the inputs are selected by the LMAS field from the local control field associated with the processor P1 provided from the control store 36 as discussed above with respect to Table 5. One of the inputs to the multiplexer 80 is provided by the LMA field from the

local control field associated with the processor P1 whereby the local memory 24 may be addressed directly under micro program control. A second input to the multiplexer 80 is provided from a local memory address register (LMA) 81 which is loaded from the 6 least significant bits of the D bus 23 under control of the deferred action control table in the control circuits 41. Thus, in a manner to be described hereinafter, the local memory 24 may be addressed in accordance with a deferred action. The third input to the multiplexer 80 is provided from the shift/mask address PROM 70 which addresses thirty-six locations in the local memory 24 which are utilized for storing masks used in the local processor computations.

The addressed words from the local memory 24 are applied through a complementary 82 to an A latch register 83 which, in turn, provides its 40-bit input to the A port of the local processor 17. The complement 82 will be later discussed. The latches provided by the A register 43 are required since the A port of the local processor 17 is not provided with an internal latch. The B port to the local processor 17 is so provided. The selective complementation control of the complement 82 is primarily utilized in mask extraction from the local memory 24 under control of the shift/mask address PROM 70 so that 36 masks as well as their complements may be selectively provided from the local memory 24 as indicated above with respect to Tables 5 and 12.

The input, output, arithmetic and logic function control for the local processor 17 is provided by 16 function bits 50-515. In a manner to be later described in greater detail, the local processor 17 has a useful repertoire of approximately 67 functions, the 16-bit function code selecting the functions by utilizing a semi-master-bit approach. Fourteen of the 16 function bits, namely 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515 are provided from a 2 input multiplexer 84 via a function latch 85. The 2 inputs to the multiplexer 84 are provided from the control store 36 by the LPT and LPTF fields of the portion of the micro control word associated with the local processor P1. The selection of these function control fields is provided by the selection input to the multiplexer 84 from decision point 3 from the decision logic 40. Thus, in accordance with the state of DPT, either the function called for by the LPTF or that called for by LPTF will be performed by the local processor 17 in accordance with the control arrangement for the CPU 10 to be later described.

The Sg function bit of the local processor 17 controls the output of the local processor accumulator to the D port. The Sg function bit is provided from an accumulator output control multiplexer 86 via an Sg function latch 87. The 2 bits of the OUT field of the portion of the micro control word associated with the P1 processor are applied respectively to the 2 inputs to the multiplexer 86, selection therebetween being effected by the decision point 7 signal from the decision logic 40. The specific output control effected was delineated above with respect to Table 8. For reasons to be clarified, the local processor function controlled by the Sg function

	Docum ent ID	U	Title	Current OR
20	US 62893 96 B1	<input checked="" type="checkbox"/>	Dynamic programmable mode switching device driver architecture	719/323
21	US 62369 40 B1	<input checked="" type="checkbox"/>	Display monitor for golf cart yardage and information system	701/300
22	US 62363 60 B1	<input checked="" type="checkbox"/>	Golf course yardage and information system	342/357 .13
23	US 61725 21 B1	<input checked="" type="checkbox"/>	Programmable logic IC having memories for previously storing a plurality of configuration data and a method of reconfiguring same	326/40
24	US 60650 67 A	<input checked="" type="checkbox"/>	System, method and program for controlling access to an input/output device possible resource settings data in an advanced configuration and power interface operating system	710/8
25	US 60471 15 A	<input checked="" type="checkbox"/>	Method for configuring FPGA memory planes for virtual hardware computation	716/16
26	US 58783 69 A	<input checked="" type="checkbox"/>	Golf course yardage and information system	701/215
27	US 58601 33 A	<input checked="" type="checkbox"/>	Method for altering memory configuration and sizing memory modules while maintaining software code stream coherence	711/171
28	US 57520 35 A	<input checked="" type="checkbox"/>	Method for compiling and executing programs for reprogrammable instruction set accelerator	717/153
29	US 57489 79 A	<input checked="" type="checkbox"/>	Reprogrammable instruction set accelerator using a plurality of programmable execution units and an instruction page table	712/37
30	US 56894 31 A	<input checked="" type="checkbox"/>	Golf course yardage and information system	701/213
31	US 51795 30 A	<input checked="" type="checkbox"/>	Architecture for integrated concurrent vector signal processor	708/520
32	US 49891 37 A	<input checked="" type="checkbox"/>	Computer memory system	711/203
33	US 49673 40 A	<input checked="" type="checkbox"/>	Adaptive processing system having an array of individually configurable processing components	712/19
34	US 47759 32 A	<input checked="" type="checkbox"/>	Computer memory system with parallel garbage collection independent from an associated user processor	707/206

bit is not utilized in the operation of the CPU 10 and the function is disabled by applying a permanent "1" signal to the S4 input. The components 80, 82-87 may for convenience be designated as a block 88.

Associated with the local processor 18 and local memory 25 is a block 88' and associated with the local processor 19 and the local memory 26 is a block 88". The blocks 88' and 88" are identical to the block 88 with the exception that appropriately associated local control fields from the control store 36 are applied thereto. The local memory address register 81 and the shift/mask address ROM 70 provide inputs to the blocks 88' and 88" for reasons similar to those discussed with respect to the block 88.

The local processor 27 with its associated local memory 28 is configured somewhat differently from the processor 17, 18 and 19. The addressing of the local processor 28 has previously been discussed with respect to the blocks 63 and 64. The local processor 27 utilizes 16 function bits S0-S15 in a manner similar to that described above with respect to the processor 17. The function bits S0-3, 5-7, 9-15 are provided in parallel from a function select multiplexer 89 via a function latch 90. The 2 inputs to the multiplexer 89 are provided from the control store 36 by the local processor function fields L.P.F.T. and L.P.F.F. from the portion of the micro control word associated with the P4 processor as discussed above with respect to FIG. 4. The selection between L.P.F.T. and L.P.F.F. is effected by decision point 6 from the decision logic 40. The carry in (CIN) input to the processor 27 is treated as a function bit and is provided from one of the function bit outputs of the multiplexer 89. The S6 input is permanently enabled by a 1 input since the processor 27 utilizes the private D4 bus 30 to which it exclusively provides inputs. The S4 input to the processor 27 is permanently disabled in the manner and for the reasons discussed above with respect to the processor 17.

Each of the local processors 17, 18, 19 and 27 are preferably constructed from LSI chips of the micro processor variety. Particularly, the Motorola 10,800 4-bit slice ALU was selected for the implementation. The detailed specifications for this ALU slice may be found in the publication entitled "M10800-HIGH PERFORMANCE MCCL LSI PROCESSOR FAMILY", available from Motorola Semiconductor Products, Inc. It should be noted that the terminology utilized herein, namely, A bus, B bus and D bus, corresponds to the Motorola terminology A bus, O bus and I bus respectively.

Referring now to FIG. 6, a schematic block diagram of the ALU slice utilized to implement the local processors 17, 18, 19, and 27 is utilized depicting the components and paths that are utilized in the CPU 10. The input from the A register 83 (FIG. 5) to the A port is applied as an input to a multiplexer 100 whose output is applied to the ALU 101 of the chip as well as to a mask network 102. Another input to the mask network 102 is provided from a B bus latch 103 utilized to latch values from the B bus 22 (FIG. 5) at the beginning of each micro cycle. The output of the mask network 102 as well as the output from the latch 103 provide inputs to the ALU block 101. The ALU 101 receives the 16 function select bits S0-S15 as discussed above as well as a carry in signal. The ALU 101 also provides carry generate (G), carry propagate (P), as well as overflow and carry out signals.

The output from the ALU 101 is applied to a 1-bit shift register 104 whose output is applied to a micro accumulator 105 (designated as a) whose output, in turn, provides the value to the output D port of the processor. The output of the accumulator 105 is also applied as an input to the A bus multiplexer 100, the B bus latch 103 and the ALU 101. The shift register 104 includes a bi-directional port for the least significant bit (LSB) as well as a bi-directional port for the most significant bit (MSB) and also provides a ZERO detect output utilized as a dynamic variable in the CPU 10 which provides an indication when all of the bits transmitted through the shift register are 0.

The chip illustrated in FIG. 6 provides Boolean logic functions, binary arithmetic and a set of data routing functions, the chip having a repertoire of approximately 67 functions. As discussed above, the functions are selected by the semi-master-bitted inputs S0-S15. As previously described, the D port output can be disabled by the function bit S6 permitting the wired OR output to the D bus 23. The basic arithmetic repertoire is add, subtract, complement, shift 1 bit and the basic logic repertoire is AND, OR, EXCLUSIVE OR and NOT. Additionally, the chip can perform a Boolean logic function followed by an arithmetic function in the same micro cycle utilizing the mask network 102. Since the shift 104 is constrained to a 1-bit shift per cycle, the external high speed shifter 35 is utilized as described with respect to FIGS. 2 and 5. Data from the B bus 22 is latched in the B bus latch 103 at the beginning of each micro cycle and the result of the last operation is latched in the accumulator 105 at the end of a cycle. Since there is no internal latch for the A port of the chip, the external A register 83 is utilized to provide this capability. The complete repertoire for the chip as well as the details of its structure and operation are documented in said Motorola specification referenced above. Each of the chips utilized is 4-bit wide and is sliced parallel to the data flow. The chip is expanded to the 40-bits required by the processors 17, 18 and 19 and to the 20-bits required by the processor 27, in implementing the circuits in parallel. Specifically, in implementing the local processors 17, 18 and 19, 10 4-bit wide chips such as illustrated in FIG. 6 are utilized with the resulting 40-bit wide A, B, and D ports connected in parallel to the 40-bit wide A bus register 83, B bus 22 and D bus 23 respectively. The local processor 27 is comprised of 5 such chips with the resulting 20-bit wide A, B, and D ports being connected in parallel to the 20-bit wide A bus, B bus 28, B4 bus 29 and D4 bus 30, respectively. For each of the local processors 17, 18, 19 and 27, the function control bits S0-S15 are applied in parallel to all of the chips comprising a processor. The shifter circuits 104 for all of the chips in a processor are serially connected with respect to each other with the MSB shifter output of a chip connected to the LSB of the next higher order chip. The ZERO detect output from the chips comprising a processor are ANDed together to provide the ZERO detect dynamic variable for the processor as delineated above with respect to Table 4. The overflow outputs from the most significant chips of the respective processors 17, 18, 19 and 27 provide inputs to the decision logic 40 as variables into decision logic circuits to be described hereinafter.

As previously described, the 10 4-bit chips comprising each of the local processors 17, 18 and 19 may be utilized interconnected in a 36-bit mode or as 2, 20-bit processors in the 2X20 bit mode. The connections of